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1 The design of dynamically reconfigurable datapath coprocessors

Zhining Huang, Sharad Malik, Nahri Moreano, Guido Araujo

May 2004 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Issue 2

Full text available: pdf(467.82 KB) Additional Information: full citation, abstract, references, index terms

Increasing nonrecurring engineering and mask costs are making it harder to turn to hardwired application specific integrated circuit (ASIC) solutions for high-performance applications. The volume required to amortize these high costs has been increasing, making it increasingly expensive to afford ASIC solutions for medium-volume products. This has led to designers seeking programmable solutions of varying sorts using these so-called programmable platforms. These programmable platforms span a lar ...

Keywords: Loop pipelining, coarse-grain reconfigurable fabric, datapath synthesis, interconnection design, reconfigurable datapath

2 Modeling and validation of pipeline specifications

Prabhat Mishra, Nikil Dutt

February 2004 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Issue 1

Full text available: pdf(198.92 KB) Additional Information: full citation, abstract, references, index terms

Verification is one of the most complex and expensive tasks in the current Systems-on-Chip design process. Many existing approaches employ a bottom-up approach to pipeline validation, where the functionality of an existing pipelined processor is, in essence, reverse-engineered from its RT-level implementation. Our validation technique is complementary to these bottom-up approaches. Our approach leverages the system architect's knowledge about the behavior of the pipelined architecture, through a ...

Keywords: Modeling of processor pipeline, architecture description language, pipeline validation, pipelined processor specification

3 The effect on RISC performance of register set size and structure versus code generation strategy

David G. Bradlee, Susan J. Eggers, Robert R. Henry

April 1991 **ACM SIGARCH Computer Architecture News , Proceedings of the 18th annual international symposium on Computer architecture**, Volume 19 Issue 3

Full text available: pdf(1.07 MB) Additional Information: full citation, references, citings, index terms

4 VAX vector architecture
Dileep Bhandarkar, Richard Brunner
May 1990 **ACM SIGARCH Computer Architecture News , Proceedings of the 17th annual international symposium on Computer Architecture**, Volume 18 Issue 3
Full text available: pdf(1.14 MB) Additional Information: full citation, abstract, references, citings, index terms

The VAX Architecture has been extended to include an integrated, register-based vector processor. This extension allows both high-end and low-end implementations and can be supported with only small changes by VAX/VMS and VAX/ULTRIX operating systems. The extension is effectively exploited by the new vectorizing capabilities of VAX FORTRAN. Features of the VAX Vector Architecture and the design decisions which make it a consistent extension of the VAX Architecture are discussed.

5 Anatomy of a message in the Alewife multiprocessor
John Kubiatowicz, Anant Agarwal
August 1993 **Proceedings of the 7th international conference on Supercomputing**
Full text available: pdf(1.36 MB) Additional Information: full citation, abstract, references, citings, index terms

Shared-memory provides a uniform and attractive mechanism for communication. For efficiency, it is often implemented with a layer of interpretive hardware on top of a message-passing communications network. This interpretive layer is responsible for data location, data movement, and cache coherence. It uses patterns of communication that benefit common programming styles, but which are only heuristics. This suggests that certain styles of communication may benefit from direct access to the ...

6 A parallel pipelined data flow coprocessor
J. T. Canning, R. Miner
February 1989 **Proceedings of the seventeenth annual ACM conference on Computer science : Computing trends in the 1990's: Computing trends in the 1990's**
Full text available: pdf(594.17 KB) Additional Information: full citation, abstract, references, citings, index terms

A parallel pipelined data flow coprocessor has been developed for the 68000 based Commodore Amiga workstation. The coprocessor, based on Nippon Electric Corporation's &mgr;PD7281 Image Pipelined Processor (ImPP), was designed as an algorithm processor for numerically intensive applications such as image processing, image synthesis, and numerical analysis. The coprocessor can accomodate up to seven of the 5-MIPS ImPP's providing over 30 MIPS of processing power to dedicated ...

7 Register traffic analysis for streamlining inter-operation communication in fine-grain parallel processors
Manoj Franklin, Gurindar S. Sohi
December 1992 **ACM SIGMICRO Newsletter , Proceedings of the 25th annual international symposium on Microarchitecture**, Volume 23 Issue 1-2
Full text available: pdf(1.31 MB) Additional Information: full citation, references, citings, index terms

8 Automatic Modeling and Validation of Pipeline Specifications driven by an Architecture Description Language
Prabhat Mishra, Ashok Halambi, Peter Grun, Nikil Dutt, Alex Nicolau, Hiroyuki Tomiyama
January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**
Full text available: pdf(189.15 KB) Publisher Site Additional Information: full citation, abstract

Verification is one of the most complex and expensive tasks in the current Systems-on-Chip (SOC) design process. Many existing approaches employ a bottom-up approach to pipeline

validation, where the functionality of an existing pipelined processor is, in essence, reverse-engineered from its RT-level implementation. Our approach leverages the system architect's knowledge about the behavior of the pipelined architecture, through Architecture Description Language (ADL) constructs, and thus allows ...

Keywords: Architecture Description Language, Pipeline Verification

9 A tightly-coupled processor-network interface
Dana S. Henry, Christopher F. Joerg
September 1992 **ACM SIGPLAN Notices , Proceedings of the fifth international conference on Architectural support for programming languages and operating systems**, Volume 27 Issue 9
Full text available: pdf(1.41 MB) Additional Information: full citation, references, citings, index terms

10 Integrating message-passing and shared-memory: early experience
David Kranz, Kirk Johnson, Anant Agarwal, John Kubiatowicz, Beng-Hong Lim
July 1993 **ACM SIGPLAN Notices , Proceedings of the fourth ACM SIGPLAN symposium on Principles and practice of parallel programming**, Volume 28 Issue 7
Full text available: pdf(1.12 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper discusses some of the issues involved in implementing a shared-address space programming model on large-scale, distributed-memory multiprocessors. While such a programming model can be implemented on both shared-memory and message-passing architectures, we argue that the transparent, coherent caching of global data provided by many shared-memory architectures is of crucial importance. Because message-passing mechanisms ar much more efficient than shared-memory loads and stores fo ...

11 Code compression: Reducing code size for heterogeneous-connectivity-based VLIW DSPs through synthesis of instruction set extensions
Partha Biswas, Nikil Dutt
October 2003 **Proceedings of the international conference on Compilers, architectures and synthesis for embedded systems**
Full text available: pdf(176.82 KB) Additional Information: full citation, abstract, references, index terms

VLIW DSP architectures exhibit heterogeneous connections between functional units and register files for speeding up special tasks. Such architectural characteristics can be effectively exploited through the use of complex instruction set extensions (ISEs). Although VLIWs are increasingly being used for DSP applications to achieve very high performance, such architectures are known to suffer from increased code size. This paper addresses how to generate ISEs that can result in significant code s ...

Keywords: dependence conflict graph, heterogeneous-connectivity-based DSP, instruction set architecture, instruction set extensions, restricted data dependence graph, static single assignment

12 Applications of reconfigurable computing: Exploiting operation level parallelism through dynamically reconfigurable datapaths
Zhining Huang, Sharad Malik
June 2002 **Proceedings of the 39th conference on Design automation**
Full text available: pdf(248.27 KB) Additional Information: full citation, abstract, references, citings, index terms

Increasing non-recurring engineering (NRE) and mask costs are making it harder to turn to hardwired Application Specific Integrated Circuit (ASIC) solutions for high performance applications [12]. The volume required to amortize these high costs has been increasing, making it increasingly expensive to afford ASIC solutions for medium volume products. This

has led to designers seeking programmable solutions of varying sorts using these so-called programmable platforms. These programmable platform ...

13 Embedded systems: applications, solutions and techniques (EMBS): A hardware/software kernel for system on chip designs

Andrew Morton, Wayne M. Loucks
March 2004 **Proceedings of the 2004 ACM symposium on Applied computing**

Full text available: pdf(997.76 KB) Additional Information: full citation, abstract, references

As part of the SoC design process, the application is partitioned between implementation in hardware and implementation in software. While it is customarily the application that is subject to partitioning, it is also possible to partition the software kernel. In this paper, a uniprocessor real-time kernel that implements the Earliest Deadline First (EDF) scheduling policy is partitioned. It is partitioned by moving the EDF scheduler into a coprocessor. The coprocessor size and performance are an ...

Keywords: SoC, hardware/software codesign, operating systems

14 A tool for processor instruction set design

Bruce K. Holmer
September 1994 **Proceedings of the conference on European design automation**

Full text available: pdf(718.01 KB) Additional Information: full citation, references, citings, index terms

15 System partitioning and timing analysis: Design of multi-tasking coprocessor control for Eclipse

Martijn J. Rutten, Jos T. J. van Eijndhoven, Evert-Jan D. Pol
May 2002 **Proceedings of the tenth international symposium on Hardware/software codesign**

Full text available: pdf(646.07 KB) Additional Information: full citation, abstract, references, index terms

Eclipse defines a heterogeneous multiprocessor architecture template for data-dependent stream processing. Intended as a scalable and flexible subsystem of forthcoming media-processing systems-on-a-chip, Eclipse combines application configuration flexibility with the efficiency of function-specific hardware, or coprocessors. To facilitate reuse, Eclipse separates coprocessor *functionality* from generic support that addresses multi-tasking, inter-task synchronization, and data transport. Fi ...

16 A practical tool box for system level communication synthesis

Denis Hommais, Frédéric Pétrot, Ivan Augé
April 2001 **Proceedings of the ninth international symposium on Hardware/software codesign**

Full text available: pdf(505.13 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a practical approach to communication synthesis for hardware/software system specified as tasks communicating through lossless blocking channels. It relies on a limited set of templates that characterize the way data are exchanged between tasks realized either in software or in hardware. The templates are highly portable because their software part is implemented using the POSIX thread functions, and their hardware part is a hand crafted synthesizable module with a System ...

17 Architectural and organizational tradeoffs in the design of the MultiTitan CPU

N. P. Jouppi
April 1989 **ACM SIGARCH Computer Architecture News , Proceedings of the 16th annual international symposium on Computer architecture**, Volume 17 Issue 3

Full text available: pdf(1.32 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes the architectural and organizational tradeoffs made during the design of the MultiTitan, and provides data supporting the decisions made. These decisions covered the entire space of processor design, from the instruction set and virtual memory architecture through the pipeline and organization of the machine. In particular, some of the tradeoffs involved the use of an on-chip instruction cache with off-chip TLB and floating-point unit, the use of direct-mapped instead o ...

18 StaCS: a Static Control Superscalar architecture

Benoît Dupont de Dinechin

December 1992 **ACM SIGMICRO Newsletter , Proceedings of the 25th annual international symposium on Microarchitecture**, Volume 23 Issue 1-2

Full text available: pdf(1.34 MB) Additional Information: full citation, references, index terms

19 The role of VHDL within the TOSCA hardware/software codesign framework

Donatella Sciuto, Stefano Antoniazzi, Alessandro Balboni, William Fornaciari

September 1994 **Proceedings of the conference on European design automation**

Full text available: pdf(630.15 KB) Additional Information: full citation, references, citings, index terms

20 A unified vector/scalar floating-point architecture

N. P. Jouppi, J. Bertoni, D. W. Wall

April 1989 **ACM SIGARCH Computer Architecture News , Proceedings of the third international conference on Architectural support for programming languages and operating systems**, Volume 17 Issue 2

Full text available: pdf(1.25 MB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we present a unified approach to vector and scalar computation, using a single register file for both scalar operands and vector elements. The goal of this architecture is to yield improved scalar performance while broadening the range of vectorizable applications. For example, reduction operations and recurrences can be expressed in vector form in this architecture. This approach results in greater overall performance for most applications than does the approach of emphasizin ...

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